Statement of Volatility – Dell EMC PowerEdge - R7515

Dell PowerEdge R7515 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge R7515 server.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
Planer				
CPU Internal CMOS RAM	Non-Volatile	1	CPU0	256M bytes
BIOS SPI Flash	Non-Volatile	1	J6_1	32 MB
iDRAC SPI Flash	Non-Volatile	1	J5_1	4 MB
BMC EMMC	Non-Volatile	1	U_EMMC2	8 GB
System CPLD RAM	Volatile	1	U_CPLD1	34 KB
System Memory	Volatile	1	CPU0: A1~A16,	Up to 64GB per DIMM (RDIMM) Up to 128GB per DIMM (LRDIMM)
CPU Vcore and VDDCR SOC FW	Non-Volatile	1	PAAU1 PBAU1	
MEM_VDDQ FW	Non-Volatile	1	PAEU1, PBEU1	
LOM NVRAM	Non-Volatile	1	U_LOM1_ROM	8MB
Power Supplies				
PSU FW	Non-Volatile	1 per PSU	Varies by part number	Up to 2MB. Varies by part number
8x3.5'' Backplane				
SEP internal EEPROM	Non-Volatile	1	U_SEP1	Flash:64KB EEPROM:2KB

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
12x3.5'' Backplane				
t FRU image	Non-Volatile	1	U_BP_EEPROM1	EEPROM:2Kb
t FRU image	Non-Volatile	1	U_EXP_EEPROM1	EEPROM:2Kb
NVSRAM	Non-Volatile	1	U_NVSRAM1	MRAM:1Mbit
Flash	Non-Volatile	1	U_FLASH1	NOR Flash:128Mbit
24x2.5'' Backplane(12 SAS)				
t FRU image	Non-Volatile	1	U_EXP_EEPROM	EEPROM:2Kb
t FRU image	Non-Volatile	1	U12	EEPROM:2Kb
NVSRAM	Non-Volatile	1	U_NVSRAM	MRAM:1Mbit
Flash	Non-Volatile	1	U_FLASH	NOR Flash:128Mbit
24x2.5'' Backplane(24 NVME)				
t FRU image	Non-Volatile	1	U_FRU	EEPROM:2Kb
SEP internal EEPROM	Non-Volatile	1	U_SEP1	Flash:64KB EEPROM:2KB
SEP internal EEPROM	Non-Volatile	1	U_SEP2	Flash:64KB EEPROM:2KB
PERC (H330)				
NVSRAM memory	Non-Volatile	1	U1033	128KB
FRU	Non-Volatile	1	U1019	256B
1-Wire EEPROM	Non-Volatile	1	U1004	128B
SBR	Non-Volatile	1	U1020	8KB
Flash	Non-Volatile	1	U3	16MB
PERC (H740P)				
NVSRAM memory	Non-Volatile	1	U1087	128KB
FRU	Non-Volatile	1	U1019	256B
SPD	Non-Volatile	1	U22	256B
Flash	Non-Volatile	1	U1086	16MB

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
Backup Flash	Non-Volatile	1	U1100	8MB
SDRAM	Volatile	9	U1077-U1085	8GB
IDSDM				
iDSDM (uSD1, uSD2)	Non-Volatile	1	J_Ace1	Nand Flash :16GB,32GB,64GB
TPM				
Trusted Platform Module (TPM, TPM 2.0 only)	Non-Volatile	1	U_TPM	128 Bytes
BOSS				
SPI Flash	Non-Volatile	1	U17	1024KB
T-FRU	Non-Volatile	1	U7	64KB
Left (Quick Sync 2.0 module) Ear				
MCU	Non-Volatile	1	USAM7	32Mb
Left (status) Ear				
MCU	Non-Volatile	1	U_TINY	8KB
LCD Bezel				
Microcontroller	Non-Volatile	1	IC1	256KB
Right Ear				
SPI Flash	Non-Volatile	1	U2	32Mb

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
Planer			
CPU Internal CMOS RAM	Battery-backed CMOS RAM	No	Real-time clock and BIOS configuration settings
BIOS SPI Flash	SPI Flash	Yes	Boot code, system configuration information, UEFI

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
			environment, Flash Disceptor, ME
iDRAC SPI Flash	SPI Flash	No	iDRAC Uboot (bootloader), server managent persistent store (i.e. IDRAC MAC Address, iDRAC boot variables), lifecycle log cache, virtual planar FRU and EPPID, rac log, System Event Log,
BMC EMMC	eMMC NAND Flash	Yes	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware
Memory VDDQ, CPU Vcore and VSA Regulators	OTP(one time programmable)	No	Operational parameters
System CPLD RAM	RAM	No	Not utilized
System Memory	RAM	Yes	System OS RAM
Power Supplies			
Microcontroller	Flash PROM and EEPROM	Yes	Report PSU information and control firmware
12x3.5'' Backplane			
FRU	FRU	No	FRU
NVSRAM	NVSRAM	No	Configuration data
Flash	Flash	No	EXP firmware
8x3.5'' Backplane			
SEP internal EEPROM	EEPROM	No	FRU

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
24x2.5'' Backplane(12 SAS)			
FRU image	FRU	No	FRU
NVSRAM	NVSRAM	No	Configuration data
Flash	Flash	No	EXP firmware
24x2.5'' Backplane(24 NVME)			
FRU image	FRU	No	FRU
SEP internal EEPROM	EEPROM	No	FW configuration data
PERC (H330)			
NVSRAM memory	NVSRAM memory	No	Configuration data
FRU	FRU	No	Card manufacturing information
1-Wire EEPROM	1-Wire EEPROM	No	Holds default controller properties/settings
SBR	SBR	No	Boot loader
Flash	Flash	No	Card firmware
PERC (H740P)			
NVSRAM memory	NVSRAM memory	No	Configuration data
FRU	FRU	No	Card manufacturing information
SPD	SPD	No	Memory configuration data
Flash	Flash	No	Card firmware
Backup Flash	Backup Flash	No	Holds cache data during power loss
SDRAM	SDRAM	No	Cache for HDD I/O
IDSDM			

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
iDSDM (uSD1, uSD2)	NAND flash	Yes	Populate out-of-band or optionally connect to the host as mass storage and boot mechanism
TPM			
Trusted Platform Module (TPM, TPM 2.0 only)	EEPROM	Yes	Storage of encryption keys
BOSS			
SPI Flash	FLASH EEPROM	No	Boot code, FW
TFRU	FLASH EEPROM	Yes	Thermal monitoring
Left (Quick Sync 2.0 module) Ear			
MCU	embedded Flash	No	Card firmware
Left (status) Ear			
MCU	embedded Flash	No	Card firmware
LCD Bezel			
Microcontroller	Internal Flash	No	Boot loader and s/w implementation of LCD command set
Right Ear			
SPI Flash	SPI Flash	No	For field maintenance. Have License, Service Tag and system informatio

Item	How is data input to this memory?	How is this memory write protected?
Planer		
CPU Internal CMOS RAM	BIOS	N/A – BIOS only control
BIOS SPI Flash	SPI interface via iDRAC	Software write protected
iDRAC SPI Flash	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.
BMC EMMC	NAND Flash interface via iDRAC	Embedded FW write protected
Memory VDDQ, CPU Vcore and VSA Regulators	Once values are loaded into register space a cmd writes to nvm.	There are passwords for different sections of the register space
System CPLD RAM	Not utilized	Not accessible
System Memory	System OS RAM	System OS
System Memory	System OS	OS Contro
Power Supplies		
PSU FW	Different vendors have different utilities and tools to load the data to memory. It can also be loaded by Dell Update Package from LC or OS (Windows and Linux)	Protected by the embedded microcontroller. Special keys are used by special vendor provided utilities to unlock the ROM with various CRC checks during load.
12x3.5'' Backplane		
FRU	Programmed at ICT during production.	Not WP
NVSRAM	ROC writes configuration data to NVSRAM	Not WP
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP
8x3.5'' Backplane		
SEP internal EEPROM	Programmed at ICT during production	Not WP
24x2.5'' Backplane(12 SAS)		
FRU image	Programmed at ICT during production	Not WP
NVSRAM	ROC writes configuration data to	Not WP

Item	How is data input to this memory?	How is this memory write protected?
	NVSRAM	
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP
24x2.5'' Backplane(24 NVME)		
FRU image	Programmed at ICT during production	Not WP
SEP internal EEPROM	Pre-programmed before assembly. Can be updated using Dell tool.	Not WP
PERC (H330)		
NVSRAM memory	ROC writes configuration data to NVSRAM	Not WP. Not visible to Host Processor
FRU	Programmed at ICT during production	Not WP
1-Wire EEPROM	ROC writes data to this memory	Not WP. Not visible to Host Processor
SBR	Pre-programmed before assembly	Not WP. Not visible to Host Processor
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP. Not visible to Host Processor
PERC (H740P)		
NVSRAM memory	ROC writes configuration data to NVSRAM	Not WP. Not visible to Host Processor
FRU	Programmed at ICT during production	Not WP.
SPD	Pre-programmed before assembly	Not WP. Not visible to Host Processor
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP. Not visible to Host Processor
Backup Flash	FPGA backs up DDR data to this device in case of a power failure	Not WP. Not visible to Host Processor
SDRAM	ROC writes to this memory - using it as cache for data IO to HDDs	Not WP. Not visible to Host Processor
IDSDM		
iDSDM (uSD1, uSD2)	Device resides in host domain; they	(1) card may be physically removed and

Item	How is data input to this memory?	How is this memory write protected?
	are exposed to the user via an internally connected, non-removable USB mass storage device	destroyed or cleared via standard means on a separate computer OR (2)User has access to the card in the host domain and may clear it manually.
TPM		
Trusted Platform Module (TPM, TPM 2.0 only)	Using TPM Enabled operating systems	SW write protec
BOSS		
SPI Flash	By programming the image via firmware update process	N/A
TFRU	During Manufacturing, by programming the image via firmware update process. During runtime, by I2C Proprietary Command Protocol	N/A
Left (Quick Sync 2.0 module) Ear		
MCU	Pre-programmed before assembly	N/A
Left (status) Ear		
MCU	Pre-programmed before assembly	N/A
LCD Bezel		
Microcontroller	Updated as part of secure iDRAC software update. Configuration parameters can change only as part of iDRAC updat	Writes are only allowed as part of secure iDRAC update
Right Ear		
SPI Flash	SPI interface via iDRAC	Hardware strapping

NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.