Netac

Basic SO DDR4 SODIMM Memory Module Specifications

Revision History

Revision No.	History	Draft Date	Remark
1.0	Initial Release	May.2022	

Ordering Information Table

Model	Type	Capacity	Speed	Latency	Voltage
NTBSD4N32SP-16	DDR4 SODIMM	16GB	3200MHz	22-22-22-52	1.2V
NTBSD4N32SP-08	DDR4 SODIMM	8GB	3200MHz	22-22-22-52	1.2V
NTBSD4N26SP-16	DDR4 SODIMM	16GB	2666MHz	19-19-19-43	1.2V
NTBSD4N26SP-08	DDR4 SODIMM	8GB	2666MHz	19-19-19-43	1.2V
NTBSD4N26SP-04	DDR4 SODIMM	4GB	2666MHz	19-19-19-43	1.2V

Description

Netac UltraNarrow Small Outline Dual In-line Memory Module (UltraNarrow SODIMM) is a Double Data Rate Synchronous DRAM Dual In-Line Memory Modules are low power, high-speed operation memory modules that use DDR4 SDRAM devices. Each 260-pin DIMM uses gold contact fingers. The SODIMM UltraNarrow SODIMM is intended for use as main memory when installed in systems such as mobile personal computers.

Features

- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP = 2.5V (2.375V to 2.75V)
- VDDSPD=2.25V to 3.6V
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die Vref DQ generation and calibration
- On-board I²C serial presence-detect (SPD) EEPROM
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- RoHS Compliant and Halogen-Free

Pin Assignments

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VSS	2	VSS	131	A2	132	A1
3	DQ6	4	DQ4	133	A4	134	BWE#_A
5	VSS	6	VSS	135	VDD	136	VDD
7	DQ7	8	DQ5	137	CKE_A	138	CK1_A
9	VSS	10	VSS	139	CK0_A	140	CK1_C
11	DQS0_C	12	DM0_n, DBI0_n	141	VDD	142	VDD
13	DQS0_t	14	VSS	143	RAS#/A16	144	A10
15	VSS	16	DQ0	KEY			
17	DQ2	18	VSS				
19	VSS	20	DQ3	145	BA1	146	A13/WE#
21	DQ1	22	VSS	147	VDD	148	VDD
23	VSS	24	DQ12	149	CS0_n	150	BA0
25	DQ13	26	VSS	151	A14/WE_n	152	A15/RAS_n
27	VSS	28	DQ8	153	VDD	154	VDD
28	DQ9	30	VSS	155	ODT0	156	A18/CAS_n
31	VSS	32	DQS1_C	157	CS1_n	158	A17
33	DM1_n, DBI1_n	34	DQS1_t	159	VDD	160	VDD
35	VSS	36	VSS	161	ODT1	162	C0, CS2_n, NC
37	DQ15	38	DQ14	163	VDD	164	VREFCA
39	VSS	40	VSS	165	C1, CS3_n, NC	166	BA2
41	DQ11	42	DQ10	167	VSS	168	VSS
43	VSS	44	VSS	169	DQ37	170	DQ36
45	DQ21	46	DQ20	171	VSS	172	VSS
47	VSS	48	VSS	173	DQ33	174	DQ32
49	DQ17	50	DQ16	175	VSS	176	VSS
51	VSS	52	VSS	177	DQS4_C	178	DM4_n, DBI4_n
53	DQS2_C	54	DM2_n, DBI2_n	179	DQS4_t	180	VSS
55	DQS2_t	56	VSS	181	VSS	182	DQ38
57	VSS	58	DQ22	183	DQ39	184	VSS
59	DQ23	60	VSS	185	VSS	186	DQ35
61	VSS	62	DQ18	187	DQ34	188	VSS
63	DQ19	64	VSS	189	VSS	190	DQ49
65	VSS	66	DQ28	191	DQ41	192	VSS

67	DQS3	69	VSS	133	1198	134	DQ31
68	VSS	70	DQ24	135	2Q40	136	VSS
71	DQ25	72	VSS	137	VSS	138	DQ35_c
73	VSS	74	DQS3_c	139	DM5_c, DBI5_c	200	DQ29_t
75	DQ5_c, DBI3_c	76	DQS3_t	201	VSS	202	VSS
77	VSS	78	VSS	203	DQ48	204	DQ47
79	DQ27	80	DQ21	205	VSS	206	VSS
81	VSS	82	VSS	207	DQ42	208	DQ43
83	DQ23	84	DQ27	209	VSS	210	VSS
85	VSS	86	VSS	211	DQ52	212	DQ53
87	CB5, NC	88	CB4, NC	213	VSS	214	VSS
89	VSS	90	VSS	215	DQ49	216	DQ48
91	CB1, NC	92	CB0, NC	217	VSS	218	VSS
93	VSS	94	VSS	219	DQ58_c	220	DM6_c, DBI6_c
95	DQS8_c	96	DM8_c, DBI8_c	221	DQ59_t	222	VSS
97	DQS8_t	98	VSS	223	VSS	224	DQ54
98	VSS	100	CB6, NC	225	DQ55	226	VSS
101	CB2, NC	102	VSS	227	VSS	228	DQ50
103	VSS	104	CB7, NC	229	DQ51	230	VSS
105	CB3, NC	106	VSS	231	VSS	232	DQ60
107	VSS	108	RESET_n	233	2Q61	234	VSS
109	CKE0	110	CKE1	235	VSS	236	DQ57
111	VDD	112	VDD	237	DQ69	238	VSS
113	BG1	114	ACT_n	239	VSS	240	DQS7_c
115	BG0	116	ALERT_n	241	DM7_n, DBI7_n	242	DQS7_t
117	VDD	118	VDD	243	VSS	244	VSS
119	A12	120	A11	245	2Q63	246	DQ63
121	A9	122	A7	247	VSS	248	VSS
123	VDD	124	VDD	249	2Q69	250	DQ69
125	A8	126	A6	251	VSS	252	VSS
127	A5	128	A4	253	SCL	254	SDA
129	VDD	130	VDD	255	VDDSPD	256	SA0
				257	VTT	258	VTT
				259	VTT	260	SA1

NOTE: The pin assignment table above is a comprehensive list of all possible pin assignments for DDR4 SODIMM modules. See Functional Block Diagram for pins specific to this module.

Pin Descriptions

Pin Name	Description	Pin Name	Description
A0-A16	SDRAM address bus	SCL	I²C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I²C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0-SA2	I²C slave address select for SPD/TS
RAS_n/	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n/	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n/	SDRAM write enable	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	Rank Select Lines	C0, C1	Chip ID lines for SDRAM components
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0-CB7	DIMM ECC check bits		
DQS0_t-DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c-DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	SPD signals a thermal event has occurred
DM0_n-DM8_n/ DBI0_n-DBI8_n	SDRAM data mask/data bus inversion (x8-based x72 DIMMs)	VTT	Termination supply for the Address, Command and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

Notes: BA0_n is a multiplexed function with A17; CAS_n is a multiplexed function with A15; WE_n is a multiplexed function with A14.

Input/Output Functional Descriptions

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock are sampled on the crossing of the positive pin. All address and control input signals edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be

		maintained high throughout read and write accesses. Input buffers, excluding CKE, RESET_n, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1	Input	Chip ID: Chip ID is only used for 3DS for 2 and 4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, DM_n/DBI_n, and DM_n/DBI_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15, and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. These pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15, and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write, and other command defined in command truth table
DM_n/DBI_n	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is disabled with DBI function. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0-BG1	Input	Bank Group Inputs: BG0 – BG1 define which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components, only BG0 is valid.
BA0-BA1	Input	Bank Address Inputs: BA0 – BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 – A16	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A16/AR, A15/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by Bank addresses.

A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.
PARITY	Input	Command and Address Parity Input: 3DPH Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DDR4M calculates Parity with ACT_n, RAS, s/A15, CAS, s/A16, WE, s/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW.
ALERT_n	Output	ALERT_n has multiple functions, such as CRC error flag or Command and Address Parity error flag as an Output signal. If there is an error in CRC, then ALERT_n goes LOW for the period in the internal and goes back HIGH. If there is an error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. Using this signal or not is dependent on the system. This is an open drain signal. It requires a pullup resistor on the system.
EVENT_n	Output	PC thermal event indication. Open drain is required a pullup resistor on the system.
SAVE_n	Input/ Output	Not Used on SO-DIMMs. SO-DIMMs will have no connection to this pin. See specifications of NVDIMMs for signal description.
SCL	Input	Bus clock used to strobe data into and out of I2C devices. Open drain and requires a pullup resistor on the system.
SDA	Input/ Output	PC data. Open drain and requires a pullup resistor on the system.
SA0,SA2	Input	Device address for the SPD.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
NC		NC Connect. No-on DIMM electrical connection is present.
VDD	Supply	Power Supply: 1.2V +/- 0.06V
VSS	Supply	Ground.
VTT	Supply	Power Supply: 0.6V.
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min., 2.75V max.)
VREFCA	Supply	Reference voltage for CA
VDDSPD	Supply	Power supply used to power the I²C bus on the SPD.

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to V_{SS}	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to V_{SS}	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to V_{SS}	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to V_{SS}	-0.3 ~ 1.5	V	1,3,5
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ. When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV.
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5V is specified in DDR4 Device Operation.

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range	85 to 95	°C	1,3

Notes:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 ~ 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the SPD for option availability.
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or to enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

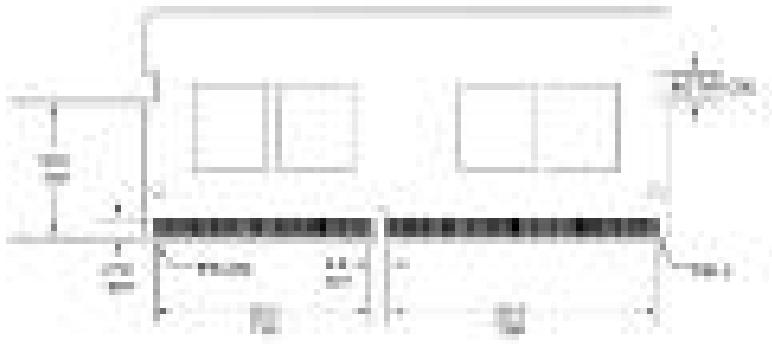
Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

Module Dimensions

Front view

Back view



Notes:

1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
2. Tolerance on all dimensions ±0.15mm unless otherwise specified.
3. This dimensional diagram is for reference only.

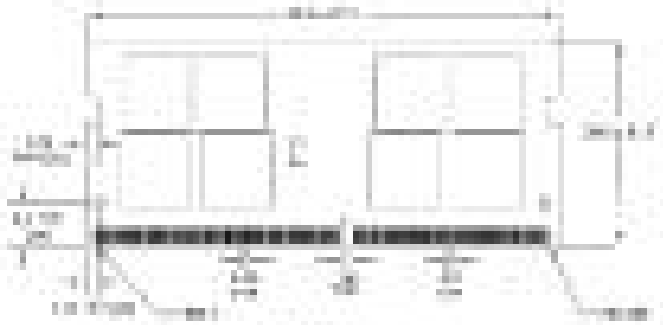
Front view

Back view

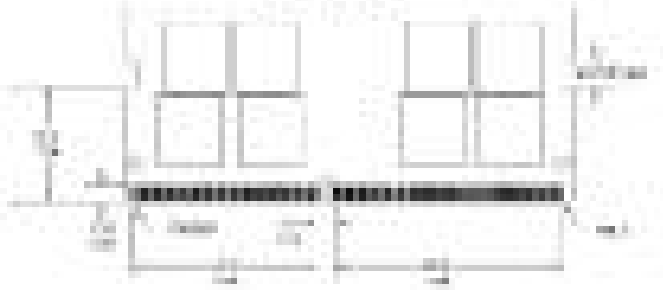
Notes:

1. All dimensions are in millimeters MM/MMN or typical (TYP) where noted.
2. Tolerance on all dimensions ±0.15mm unless otherwise specified.
3. The dimensional diagram is for reference only.

Front view



Back view



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